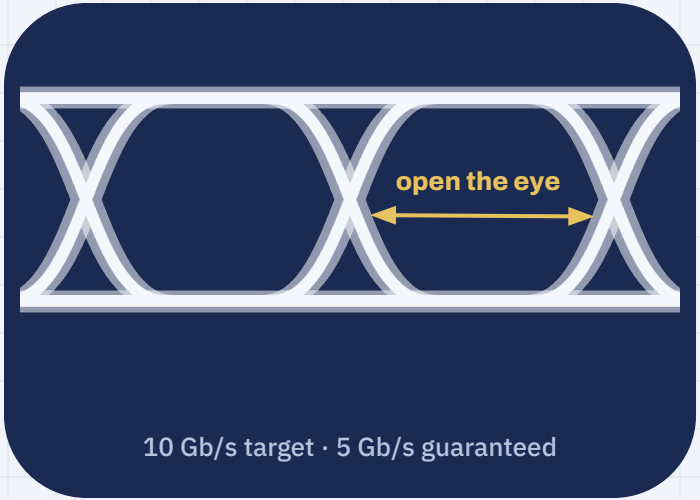
IHP SG13G2 · 130 NM SIGE BICMOS · OPEN SILICON

Open-SERDES

Towards an open-source high-speed serial link

Every fast interface rides on a SerDes, yet SerDes IP is closed. **Open-SERDES** is an **open project** to build a high-speed serial transceiver and a **reproducible channel-to-GDS flow** on open tools, for anyone to study, reuse and extend.

Tutorial: https://www.thebricd.org/serdes-tutorial/



SG13G2
IHP open PDK

FFE · CTLE
equalization

CDR
clock & data recovery

Ch → GDS
open design flow

Biomedical Research in Integrated Circuit Design
Where biomedical engineering meets IC design innovation

thebricd.org

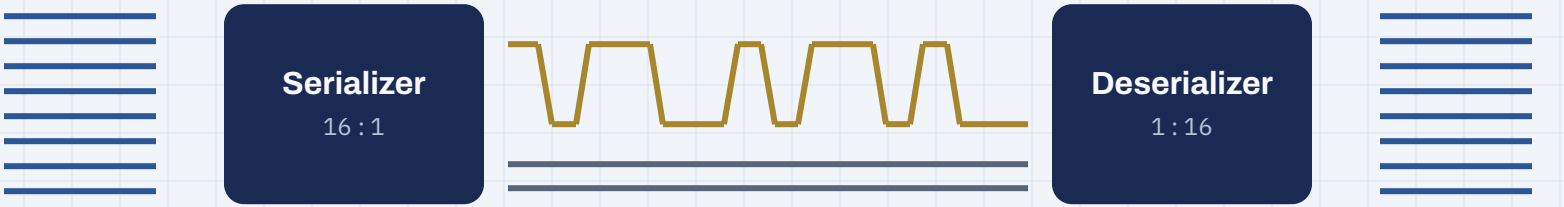
Raise your hand if...

- You used a SerDes today (USB, PCIe, Ethernet)
- You have looked at an eye diagram
- You have designed a CML gate or a StrongARM latch
- You have simulated a channel from S-parameters
- You have taped out a chip on an open PDK
- **You know an open SerDes you could tape out today**

That last hand is why we're here.

Open PDKs opened up digital and analog design. The high-speed link is still a black box.

Every fast interface is a SerDes



16 × 312.5 Mb/s in

One differential pair · 5 Gb/s NRZ

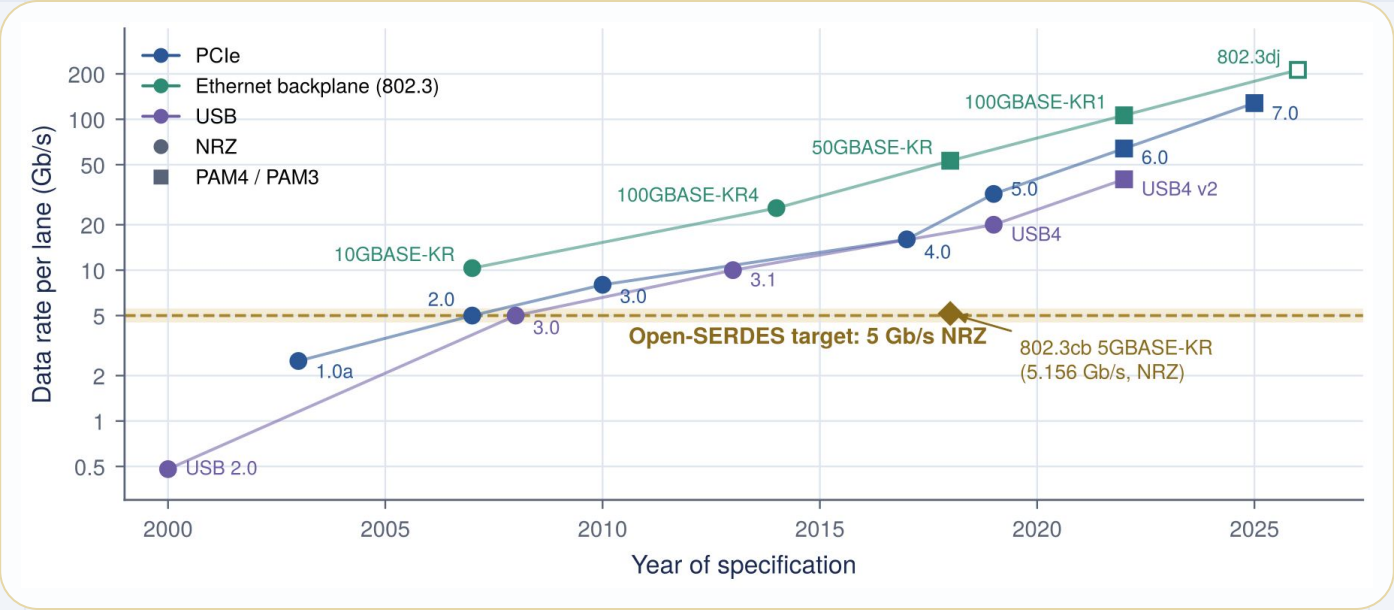
16 × 312.5 Mb/s out

Fewer pins, no skew
One differential pair with an embedded clock replaces a wide, skew-limited bus.

Everywhere
PCIe, USB, Ethernet, SATA, DisplayPort and chiplet links all ride on SerDes.

Still closed
Production SerDes IP is proprietary, NDA-bound and locked to one process.

Lane rates double every 3–4 years



Commercial lanes reach 100–200 Gb/s. Open-SERDES targets 10 Gb/s NRZ and guarantees 5 Gb/s.

From the tutorial: Figure 1.4 · thebricd.org/serdes-tutorial

What exists in the open today

Effort	What it is	Speed	What's missing
OpenSerDes (Purdue, DATE 2021)	All-digital link in SKY130 via OpenLANE; inverter TX/RX, oversampling CDR	2 Gb/s, simulated	Equalization; CMOS-speed-limited
serdespy · PyBERT · JLSD	Open Python / Julia link models: channels, FFE, CTLE, DFE, eyes	Behavioral	No tie to a PDK or real circuits
IIC-OSIC-TOOLS + SG13G2 AMS template (JKU)	Open tool container and Makefile flow to a tapeout-ready AMS chip	n/a	No high-speed link IP
Commercial SerDes IP	Silicon-proven transceivers from IP vendors and foundries	100+ Gb/s per lane	Closed, NDA, per-process licence

The gap: as far as we know, no open PDK yet has a multi-Gb/s mixed-signal transceiver with EQ and CDR, or a reproducible channel-to-GDS flow for one.

PART 1

Why IHP SG13G2?



SG13G2: a BiCMOS process built for speed

300 GHz
SiGe:C HBT transit frequency (fT)

500 GHz
HBT max. oscillation frequency (fmax)

7 metals
incl. 2 µm and 3 µm thick top Al layers

1.2 V
core CMOS, plus 3.3 V thick-oxide devices

WHAT THAT BUYS A SERIAL LINK

HBT CML with headroom
fT far above the 2.5–5 GHz Nyquist rates: fast muxes, drivers and latches.

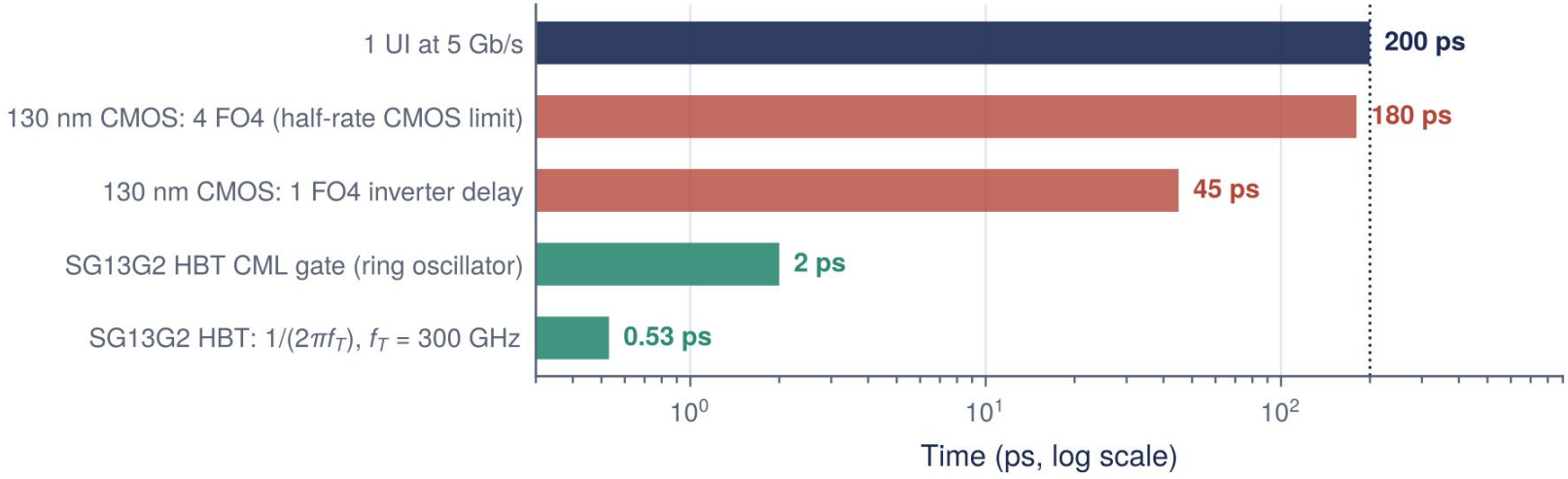
Inductors on thick metal
Shunt-peaked loads, LC-VCOs and low-loss lines on TopMetal1 and TopMetal2.

Analog-friendly passives
MIM caps, poly resistors and varactors for CTLEs, terminations and loop filters.

A real path to silicon
IHP open-source MPW runs and Tiny Tapeout IHP shuttles.

Source: IHP Open-PDK documentation, SG13G2 process specs

Why HBTs: a bit lasts four CMOS gates



CMOS runs out of margin at 5 Gb/s; an HBT gate fits 100 times per bit, still 50 at 10 Gb/s.

We don’t start from zero

OURS · SMACD 2026

2.4 GHz LC-VCO fractional-N PLL

- Fully open-source flow in SG13G2
- 4 nH spiral, Q = 16.8 (openEMS)
- −100.8 dBc/Hz at 1 MHz offset
- 12.73 mW · 0.347 mm²

UOM PROJECT · 2016

5 Gb/s SerDes model in 28 nm

- Commercial 28 nm generic library
- Fast-locking ring-VCO PLL
- Under 10 ps peak-to-peak jitter
- Architecture insight at 5 Gb/s

PURDUE · DATE 2021

OpenSerDes in SKY130

- All-digital, fully synthesizable
- OpenLANE RTL-to-GDS automation
- 2 Gb/s in post-layout simulation
- Proof that open automation works

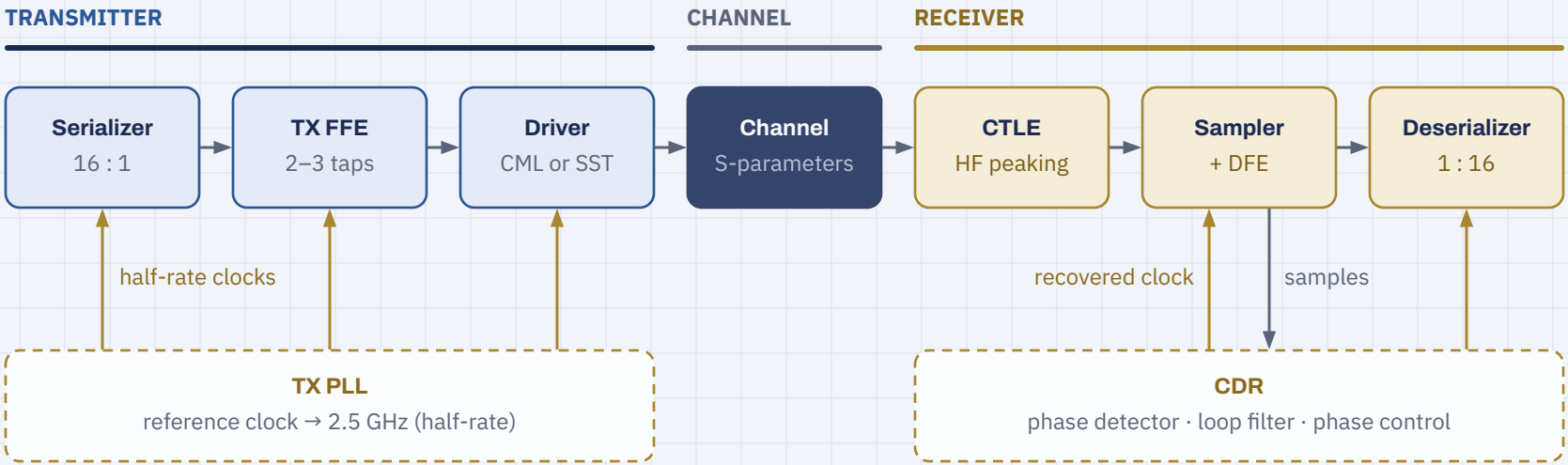
Open-SERDES = 5 Gb/s architecture insight + open automation + an open SG13G2 clock source we have already built.

PART 2

Anatomy of a Serial Link



Anatomy of a serial link



Grey arrows carry data, gold arrows carry clocks. Every box here is an open design choice; the next slides size and scope them.

5 Gb/s, in numbers

200 ps
Unit interval: each bit lasts 1 / (5 Gb/s)

2.5 GHz
Nyquist frequency the channel must carry (NRZ)

10^{-12} BER
Typical bit-error-rate target for a serial link

Same rate class as **PCIe Gen 2**, **USB 3.2 Gen 1** and **5GBASE-KR** (IEEE 802.3cb).

TO BE SET BY THE FEASIBILITY STUDY

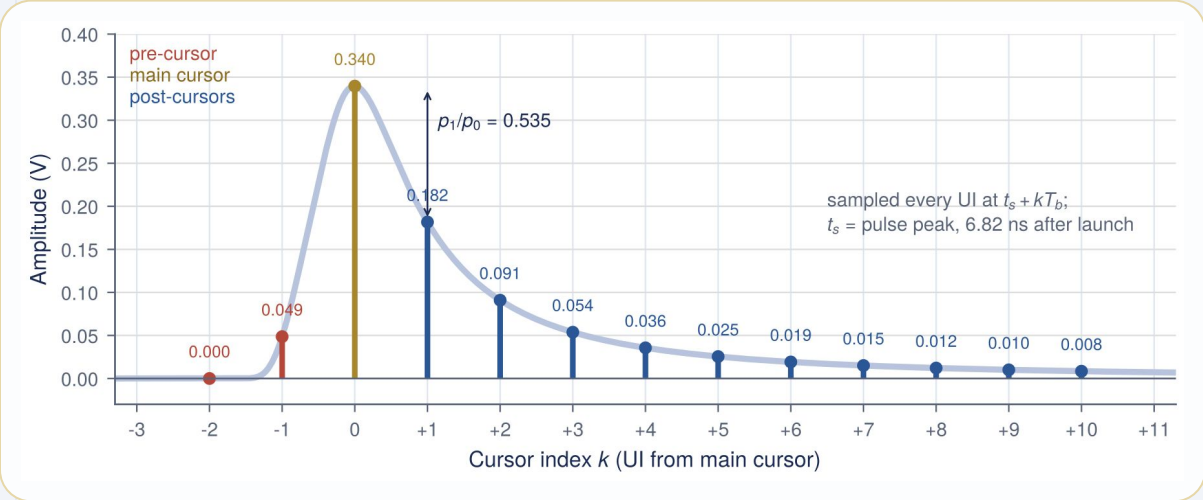
Channel loss
How much loss at 2.5 GHz must we equalize?
[__ dB]

Jitter
What total jitter can the PLL and CDR afford?
[__ ps pk-pk]

Power
Which energy per bit is competitive at 130 nm?
[__ pJ/bit]

Area
What silicon budget does one lane get?
[__ mm²]

What 1 m of FR-4 does to one bit



−17.4 dB
REF loss at the 2.5 GHz Nyquist: 1 m of FR-4 plus 300 fF pads

0.340 V
all that arrives in its own UI from a 1 V, one-UI pulse

53.5 %
first post-cursor relative to the main cursor

One bit smears over the next ten UIs: equalization must undo this inter-symbol interference.

From the tutorial: Figure 3.14 · thebricd.org/serdes-tutorial

The design space we'll explore

Modulation

NRZ PAM4

Start: NRZ; it beats PAM4 at both 5 and 10 Gb/s.

TX driver

CML (HBT) SST voltage-mode

Start: **HBT CML**; SST as the low-power follow-up.

Equalization

TX FFE **CTLE** **DFE**

Start: FFE + CTLE + 2-tap half-rate DFE; tap 1 unrolled for 10 Gb/s.

Sampler

HBT CML latch **StrongARM**

Start: **build both** and compare speed, offset and power.

Clock rate

full **half** quarter

Start: half-rate: 2.5 GHz at 5 Gb/s, 5 GHz at 10 Gb/s.

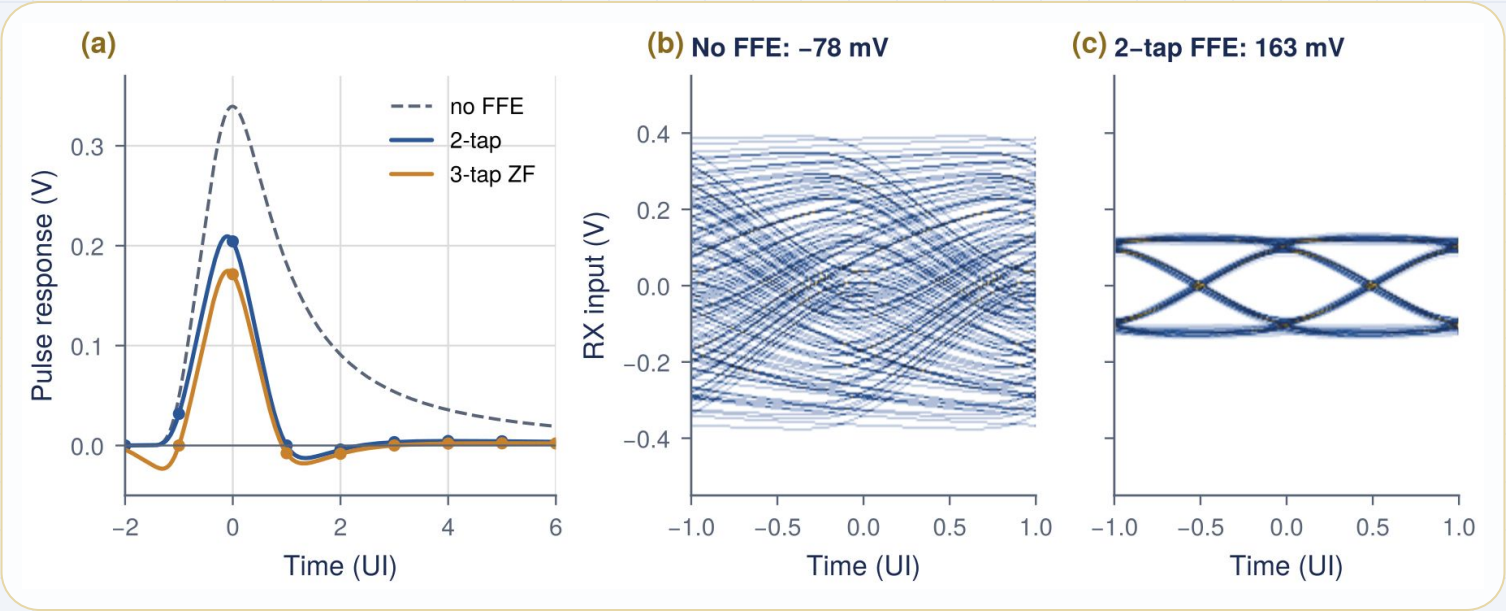
CDR

bang-bang baud-rate oversampled

Start: **bang-bang PD** with a digital loop filter.

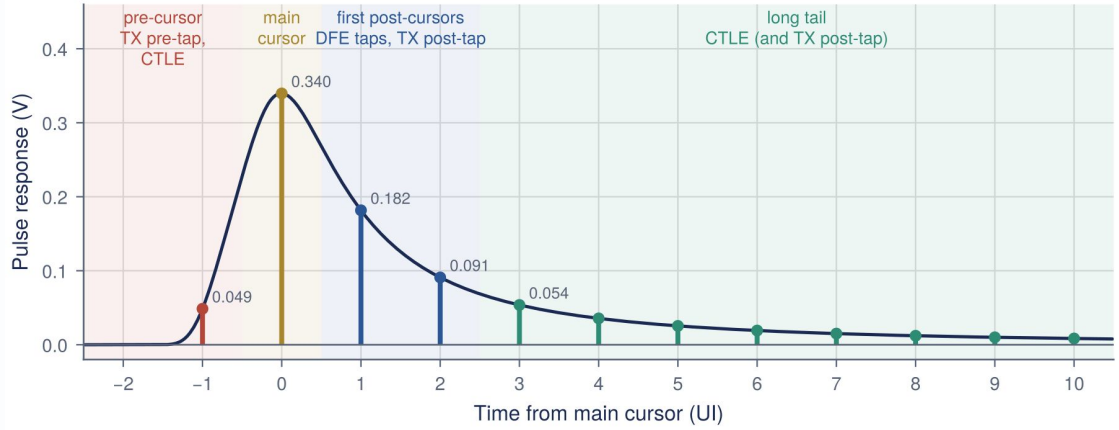
Filled pills: baseline candidates. The feasibility study makes the final call.

Equalization opens the eye



Unequalized, the REF eye is closed (−78 mV). A 2-tap TX FFE opens it to 163 mV.

Every part of the pulse has an owner



Pre-cursor
TX pre-tap or CTLE: only linear EQ can reach it

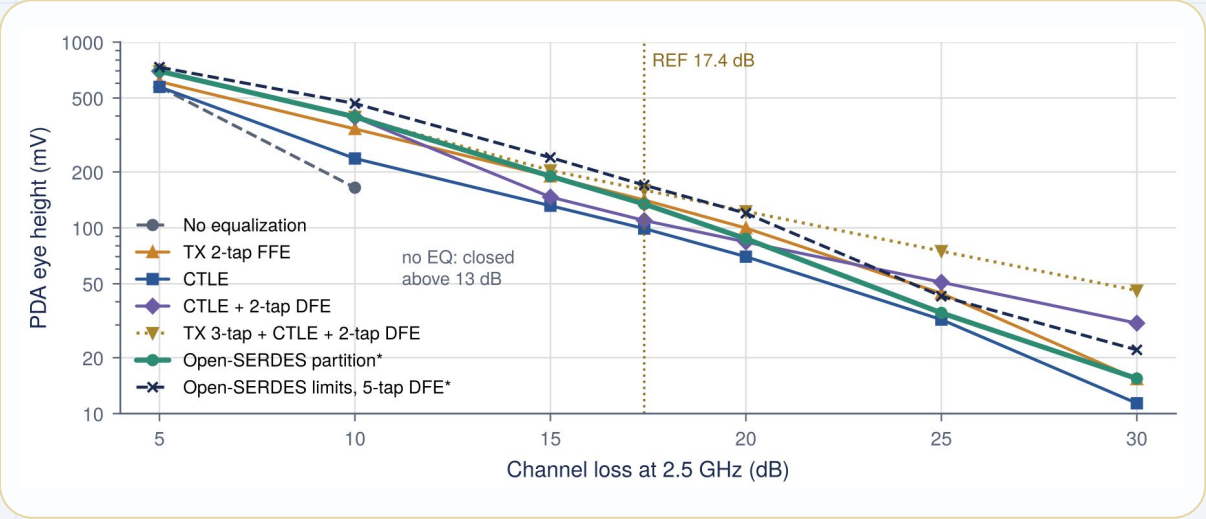
First post-cursors
DFE taps, which cancel them without adding noise

Long tail
CTLE or TX post-tap; DFE taps would need too many

Open-SERDES baseline: TX FFE + CTLE + 2-tap half-rate DFE, each on the part it does best.

From the tutorial: Figure 5.4 · thebricd.org/serdes-tutorial

Combining equalizers loses less eye



≈ 2×
eye lost per 5 dB of extra loss, for any single equalizer

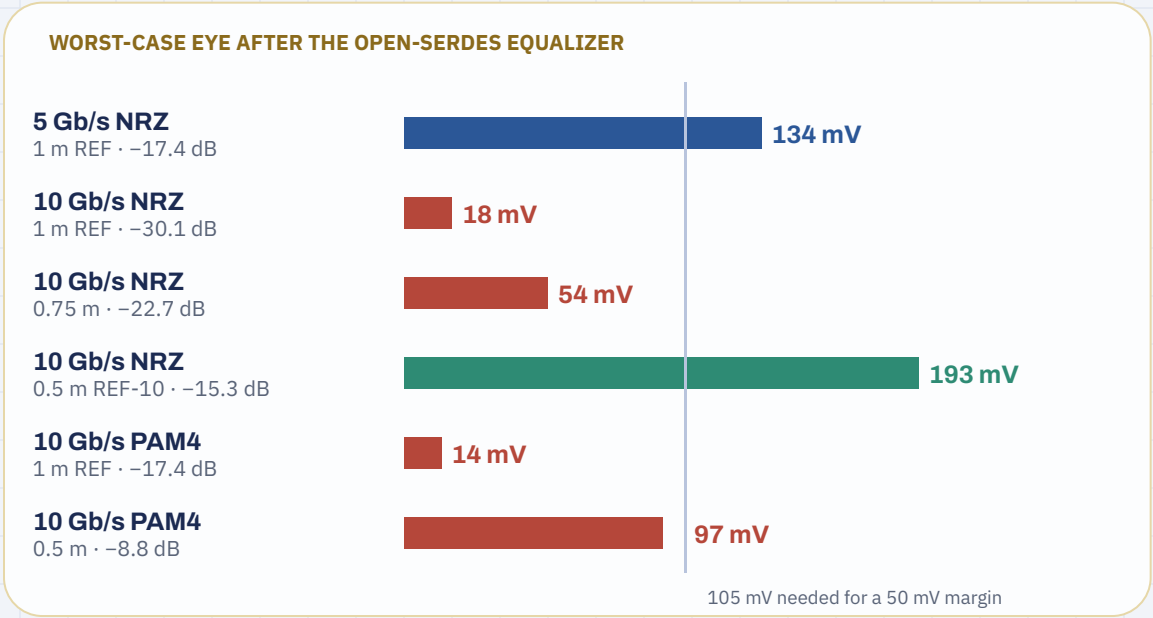
134 mV
worst-case eye on REF (17.4 dB) with the Open-SERDES partition

22 dB
where a CTLE with over 12 dB of peaking takes over

At REF the baseline leaves 134 mV, with about 4–5 dB of loss headroom before it needs more EQ.

From the tutorial: Figure 8.7 · thebricd.org/serdes-tutorial

Design for 10 Gb/s, guarantee 5



Same dB, same eye

The equalizer sees only the loss at Nyquist, not the bit rate.

REF-10

Half the REF line: 0.5 m of the same FR-4, −15.3 dB at 5 GHz.

NRZ

Beats PAM4 at both lengths, with one slicer per sample instead of three.

5 Gb/s over 1 m stays the pass criterion; 10 Gb/s over 0.5 m is the design target.

What 10 Gb/s changes

1 Clocks at 5 GHz

A 10 GHz LC VCO and a ÷2 give exact I/Q; a second ÷2 selects the 5 Gb/s mode. The polyphase filter goes away.

2 Timing budget

Same circuits: 0.46 UI of jitter. Target 0.30 UI: RJ ≤ 0.85 ps rms, DCD ≤ 4 ps, CDR dither ≤ 8 ps.

3 One more CML stage

CMOS stays at 1.25 Gb/s per lane or less: CMOS 16:8 on a 625 MHz word clock, then CML 8:4:2:1. The RX mirrors it.

4 DFE tap 1 unrolled

The ≈ 140 ps tap-1 loop is longer than the 100 ps bit, so tap 1 goes speculative: two samplers per data phase.

5 Pad and package

10 dB return loss at 5 GHz: pad ≤ 0.42 pF, so the T-coil is required; high-speed bond wires ≤ 0.5 mm.

6 Power

≈ 280 mW and ≈ 28 pJ/b, against 43 pJ/b at 5 Gb/s: CML draws its tails whatever the rate.

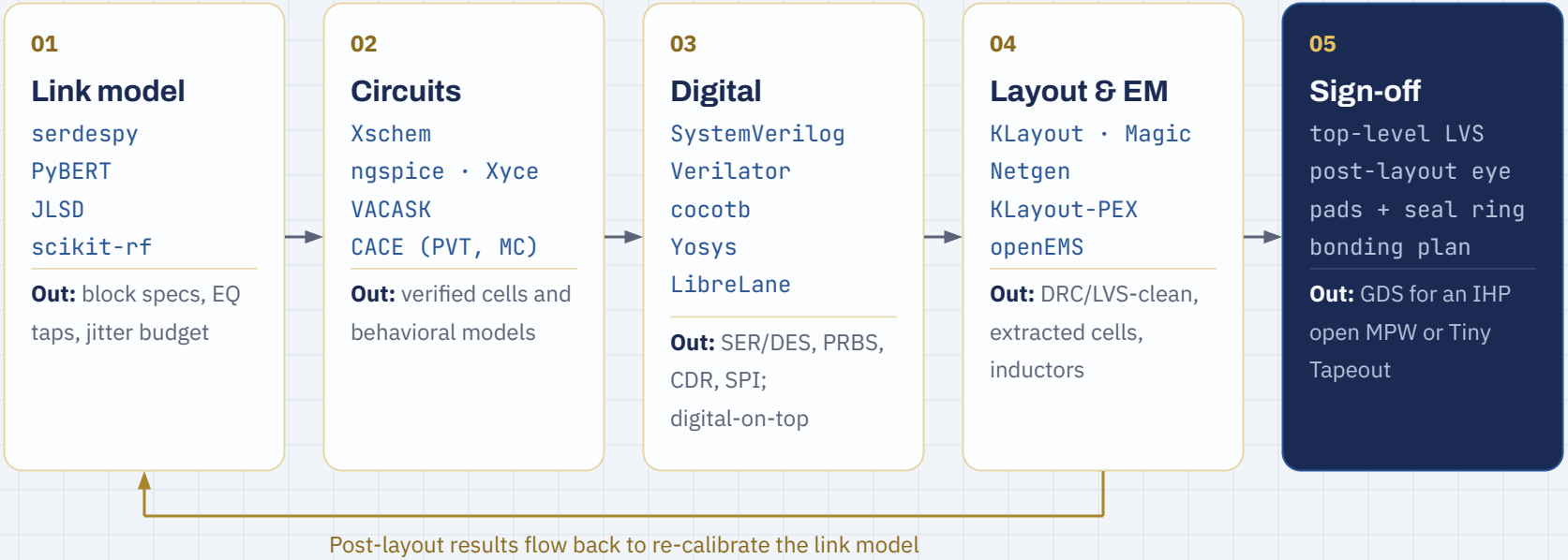
Same architecture, faster clocks: the hard part is jitter, not the transistors.

PART 3

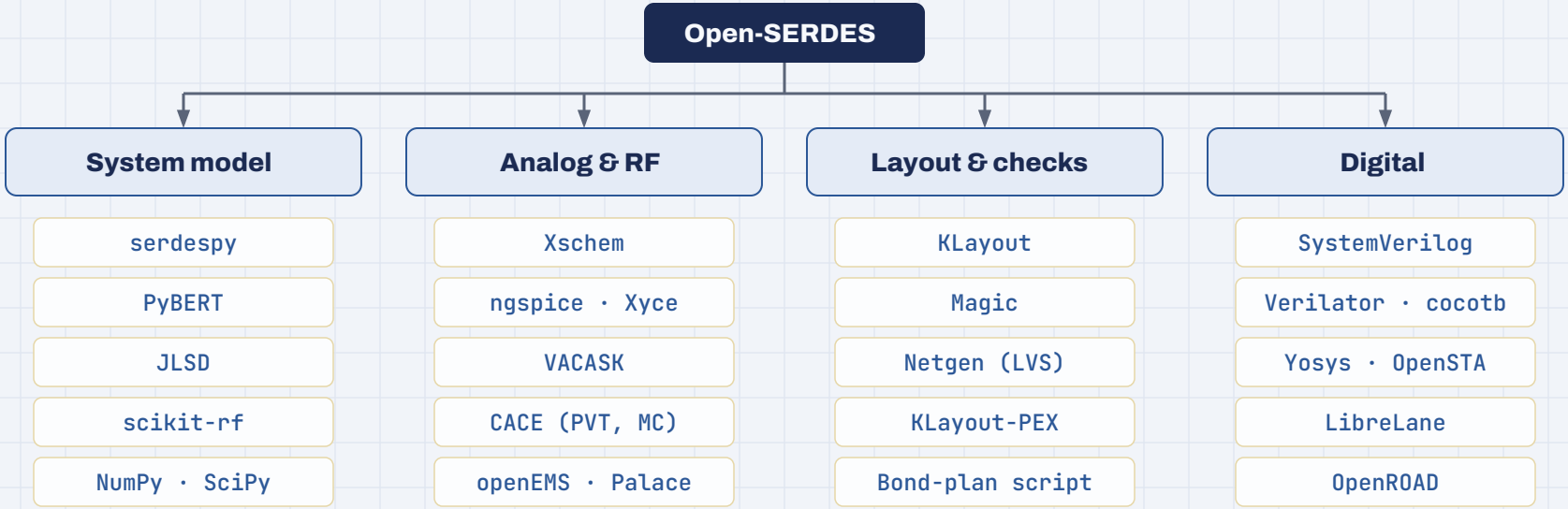
An Open Flow, Channel to GDS



The Open-SERDES flow



Tool map: every step on open tools



PDK: IHP SG13G2 Open-PDK · every tool ships in the IIC-OSIC-TOOLS container

Closing the loop: model ↔ silicon

SYSTEM

Link model

`serdespy · PyBERT · JLSD`

Channel, FFE, CTLE, DFE, CDR and jitter at the bit level

Specs: gain, peaking, swing, jitter



Extracted: pulse response, CTLE H(f), noise

CIRCUIT

SG13G2 cells

`Xschem · ngspice · Xyce`

Transistor-level and post-layout, across PVT corners

- Statistical eye and BER for every design point
- A Python GUI to explore taps and settings live
- Every number in the model traceable to a simulated cell

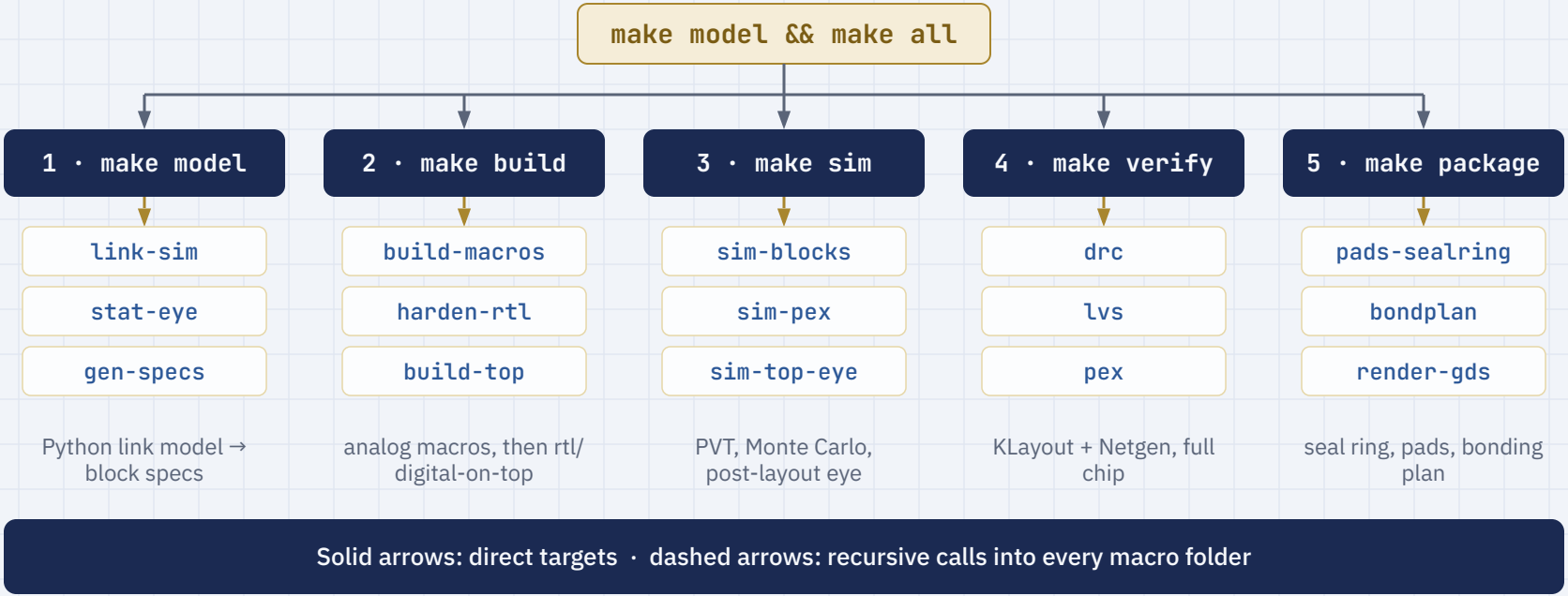
One repository, one command

- Built on JKU's **ihp-sg13g2-ams-chip-template**: Makefile-driven, recursive macros
- Each analog block is a macro with schematic, layout, testbenches and verification
- Digital logic (PRBS, SER/DES, CDR, SPI) in rtl/, hardened digital-on-top
- One spec file shared by the link model and the testbenches
- GitHub Actions regression: DRC, LVS and eye-opening checks on every commit
- Open licence throughout [MIT]

PROPOSED LAYOUT

```
open-serdes/
├ spec/                    one shared spec file
├ model/                   link model + GUI
├ channels/                S-parameter files
├ macros/                  analog, one per block
│  ├ tx_serializer/
│  ├ tx_ffe_driver/
│  ├ rx_ctle/
│  ├ rx_sampler_dfe/
│  ├ pll_lcvco/            from our SMACD PLL
│  ├ cdr_pi/               I/Q + phase interpolators
│  └ cml_lib/              shared CML cells
├ rtl/                     PRBS, SER/DES, CDR, SPI
├ verification/            regression + eye checks
├ lab/                     test board + lab data
└ Makefile
$ make model && make all
```

One command: the make targets



Why it’s hard, and why it’s worth it

THE HARD PARTS

Models at GHz
HBT compact models and parasitics must hold up at 5 GHz and beyond.

Open extraction and EM
RF-grade extraction of pads, ESD, inductors and lines is still maturing.

Jitter in simulation
PLL and CDR transients are slow, so we need calibrated behavioral models.

Packaging and test
Bondwires, a high-speed test PCB, and access to a BERT or a fast scope.

WHAT THE COMMUNITY GETS

- ✓ A first open reference design for multi-Gb/s links
- ✓ A reusable HBT / CML cell library for SG13G2
- ✓ A calibrated, open link model anyone can extend
- ✓ A teaching path from link theory to real silicon

PART 4

What We’ll Build & Test



Highlights & deliverables

HIGHLIGHTS

1. First open multi-Gb/s mixed-signal SerDes on an open PDK
2. 5/10 Gb/s NRZ transceiver: TX, RX, PLL and CDR in SG13G2
3. One reproducible flow from channel model to GDS
4. A link model calibrated against post-layout and silicon
5. Everything public: design files, models and lab data

DELIVERABLES

GDSII
tapeout-ready 5/10 Gb/s transceiver

RTL + TBs
SER/DES, PRBS, CDR logic and benches

Link model
Python simulator and GUI

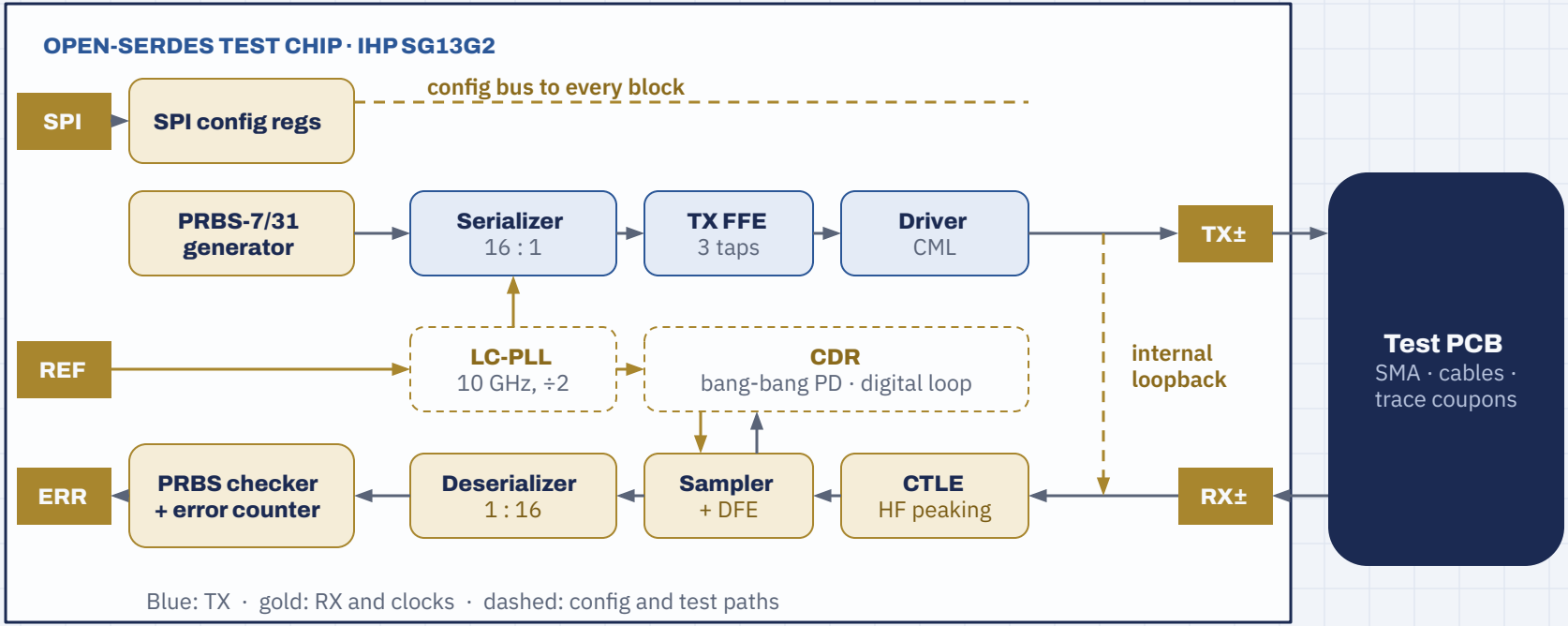
Cell library
HBT / CML cells for SG13G2

Docs
GitHub repo and tutorial

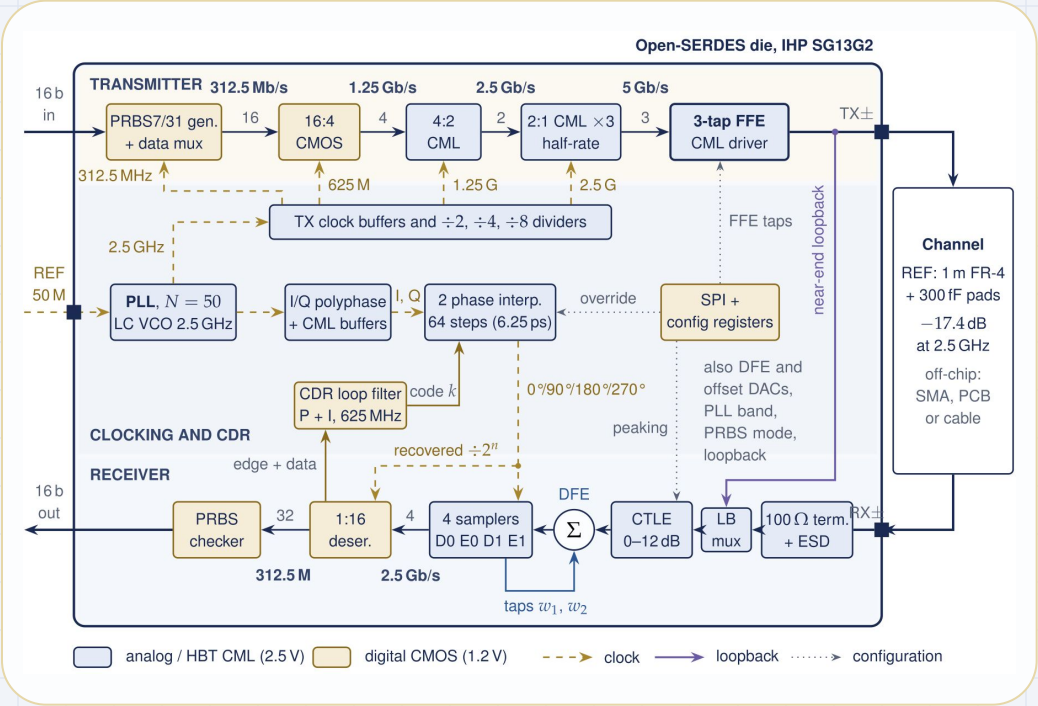
Paper + data
JSSC / TCAS, SMACD 2027, open data

Goal: clone the repo, run make all, and reproduce the chip, the models and the measurements.

Chip block diagram (concept)



The reference transceiver



16 : 1

serializer: CMOS 16:4, CML 4:2, then a half-rate 2:1

3-tap FFE

HBT CML driver, 20 mA tail, about 1 Vppd

CTLE + DFE

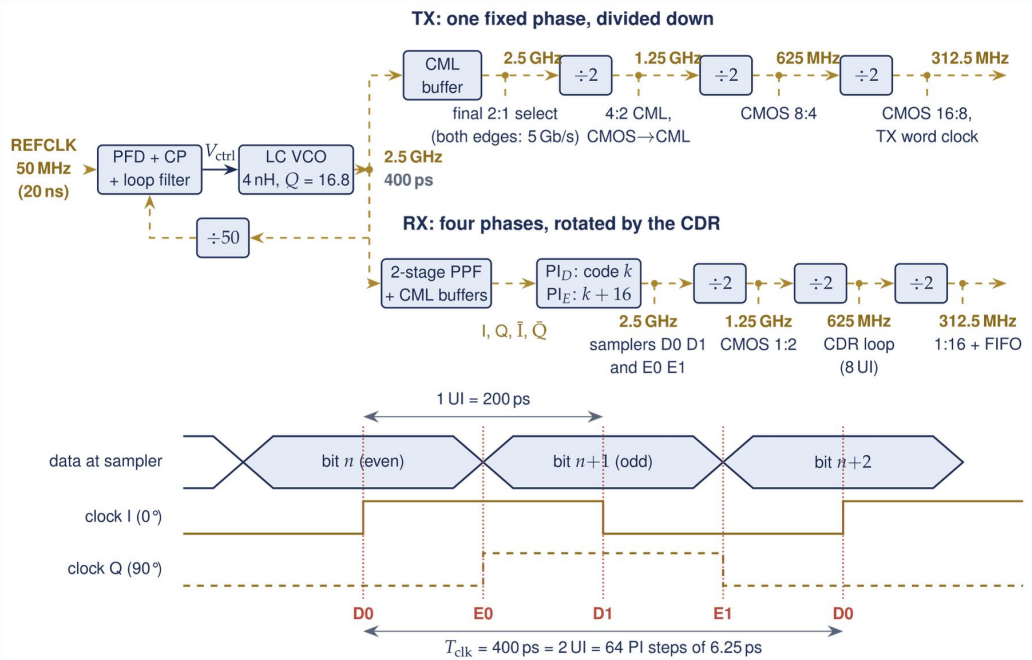
0–12 dB CTLE, 2-tap half-rate DFE, four samplers

1 PLL

2.5 GHz LC PLL, PI-based bang-bang CDR, near-end loopback

A CMOS core at 312.5 MHz, wrapped in HBT CML wherever a signal runs at 1.25 GHz or faster.

One PLL clocks the whole chip



2.5 GHz

LC-VCO PLL from a 50 MHz reference, N = 50

÷2 ÷4 ÷8

TX: one fixed phase, divided down to the 312.5 MHz word clock

64 steps

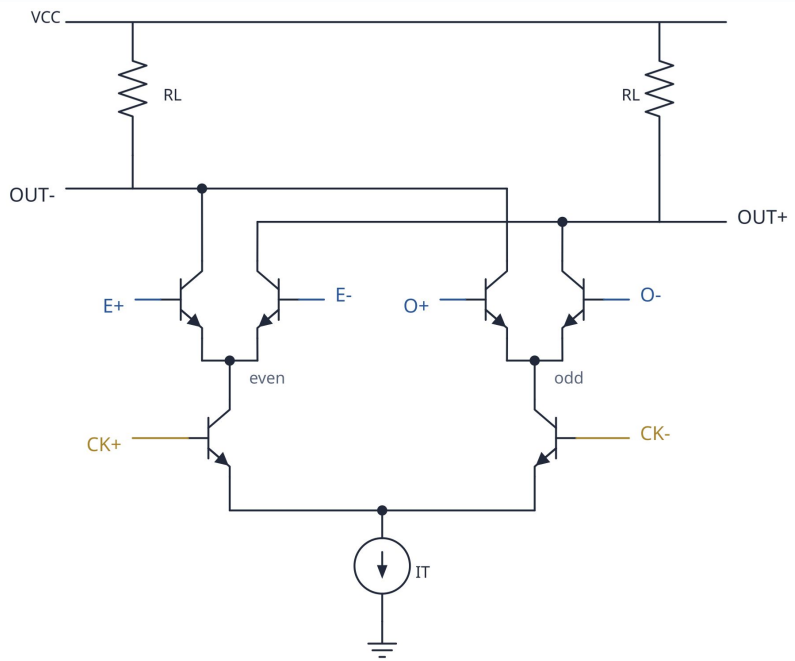
RX: polyphase I/Q rotated by two PIs, 6.25 ps per step

625 MHz

CDR loop update rate: once every 8 UI

One 400 ps clock period carries two bits.

The clock is the select in the 2:1 mux



300 mV
CML swing: RL 500 Ω times IT 0.6 mA

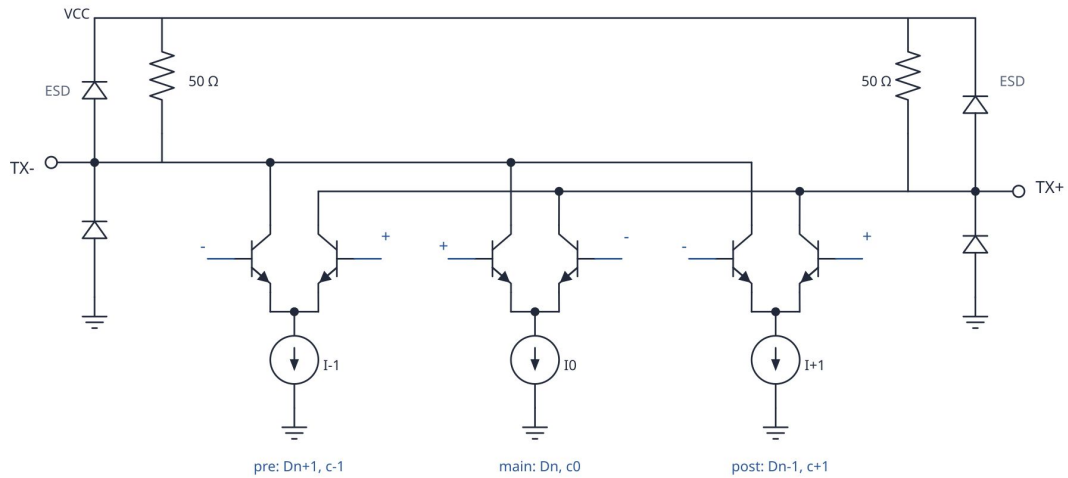
20 ps
RL·CL time constant for f3dB ≥ 7.5 GHz

×3
copies feed Dn+1, Dn and Dn−1 to the FFE taps

±100 ps
retiming window: inputs change only while deselected

A 45 % duty cycle costs 20 ps of DJ.

Three FFE taps share one 20 mA driver



1 Vppd
20 mA into 50 Ω loads that are also the back-termination

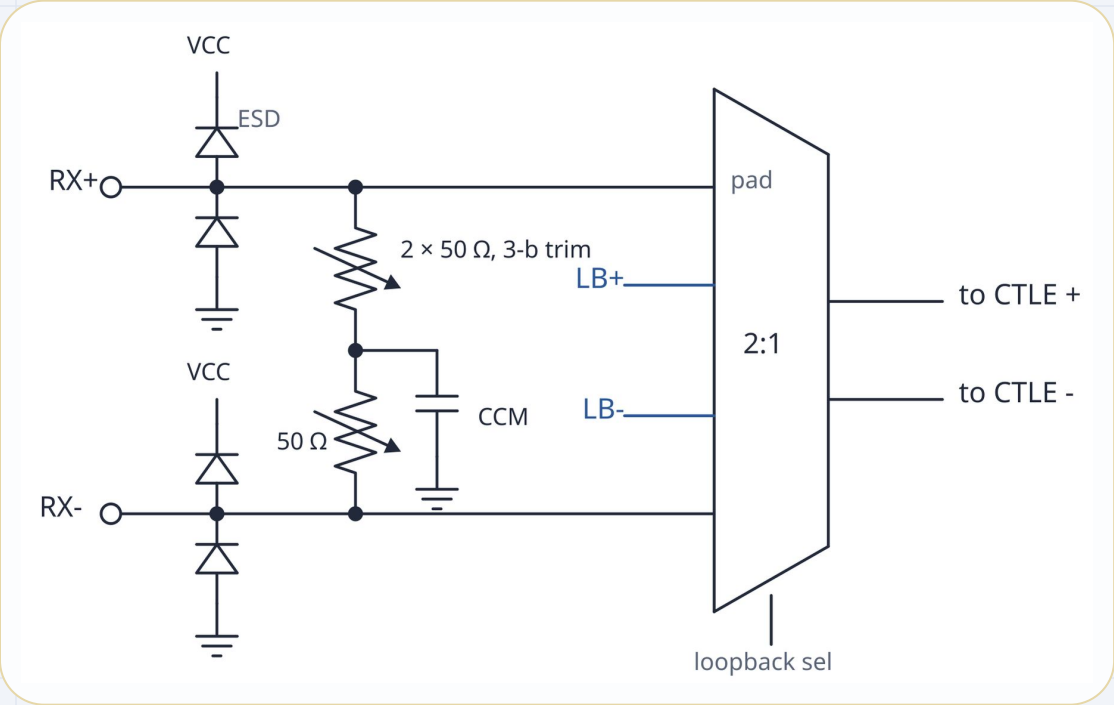
50 mW
from 2.5 V, the same at every FFE preset

32 cells
of 0.625 mA set the taps; −6 dB is 24 + 8 cells

0.85 pF
pad budget for 10 dB return loss at 2.5 GHz

Off device sits at 1.25 V; BVceo is 1.6 V.

The receiver terminates the line at the pad



19 dB
return loss even with a ±20 % resistor spread

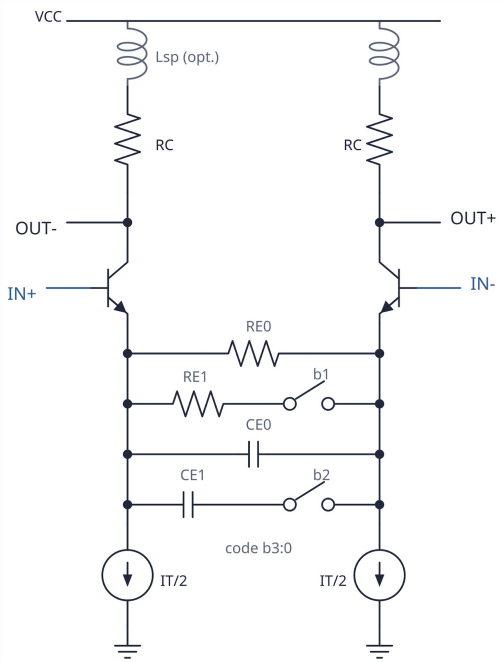
3-bit
trim on 2 × 50 Ω rppd, centre tap AC-grounded

2.0 V
DC-coupled: the RX inherits the TX common mode

2:1
CML mux selects the pad or the near-end loopback

The mux input counts against 0.85 pF.

Switched banks set 0–12 dB of CTLE peaking



0–12 dB
peaking from 4-bit RE and CE banks with MOS switches

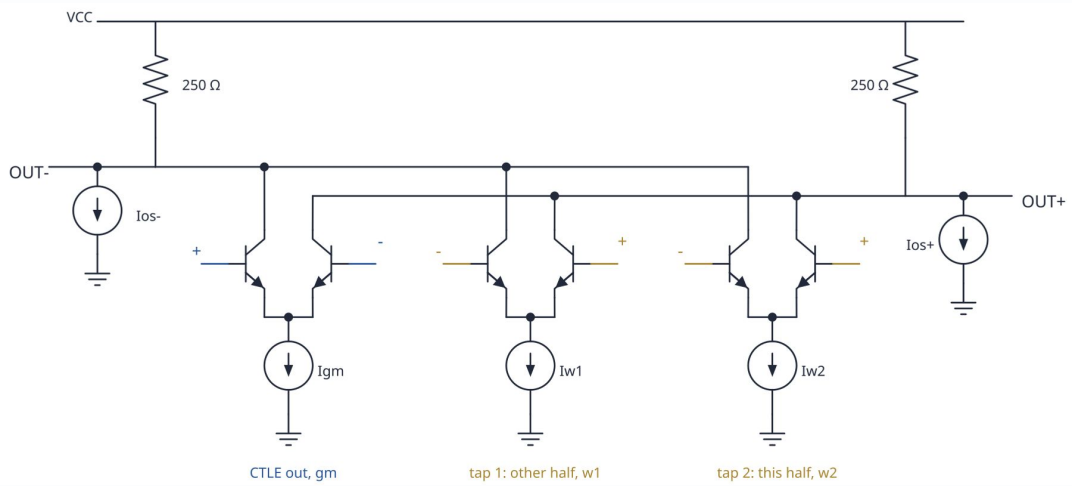
10 dB
at Nyquist with RE 317 Ω, CE 0.72 pF and IT 2 mA

7.5 GHz
minimum second pole: RC 200 Ω into about 100 fF

±0.25 V
linear input range, set by IT·RE/2

On REF the best code is 0 dB: keep it wide.

The DFE subtracts echoes as currents



140 ps

tap-1 loop: CK-to-Q, tap, settling and setup, of 200 ps

20 ps

settling τ: 250 Ω loads with about 80 fF

w1, w2

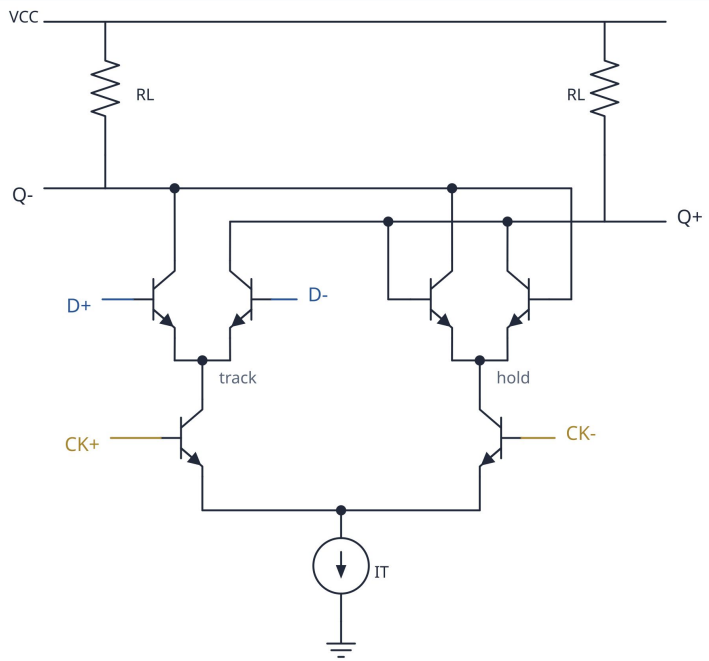
DAC tails: 0 to 0.5 and ±0.15 of the main cursor

±58 µA

5-bit offset trim injected into the same loads

Past 0.7 UI after layout: unroll tap 1.

Bipolar latches regenerate in about 4 ps



4 ps
regeneration τ with IT 1 mA, RL 400 Ω, gm·RL 7.7

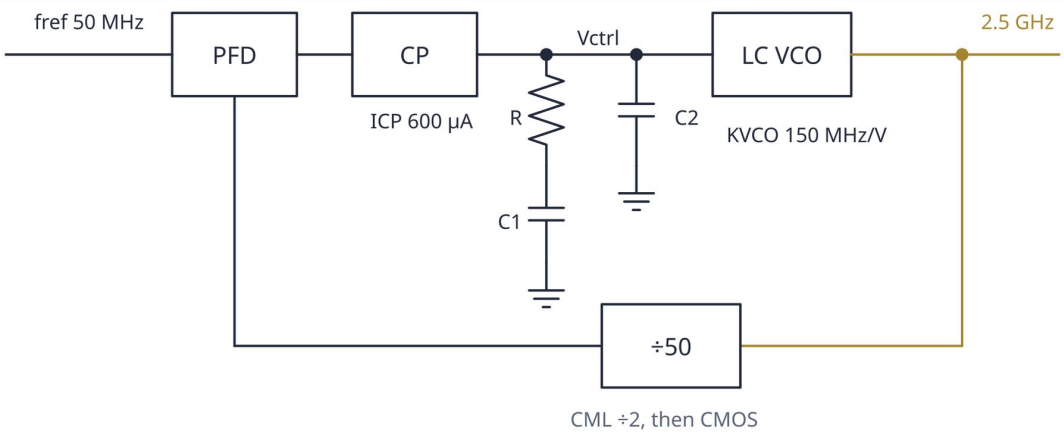
25–30 ps
aperture, matched between data and edge samplers

20 mV
sensitivity at a BER of 1e-12, σ about 1 mV

2.5 mW
per latch; two make one master–slave sampler

A StrongARM needs 100 ps: too slow here.

Our SMACD PLL, retuned to 2.5 GHz



N = 50
integer-N from a 50 MHz reference

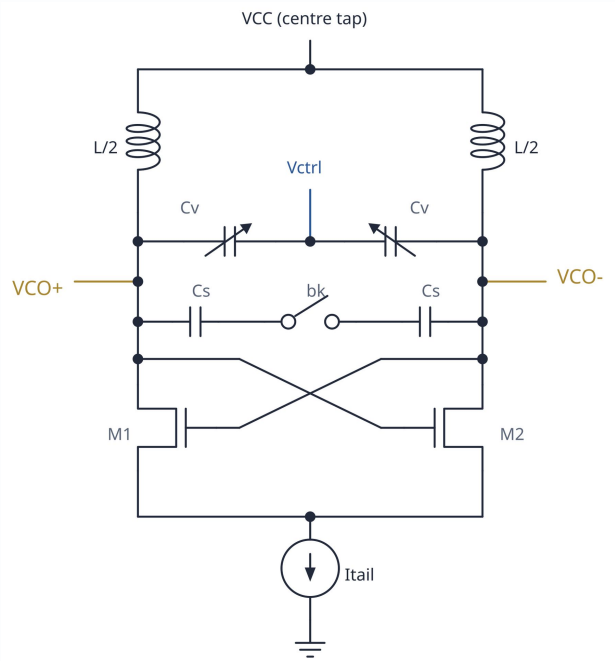
3 MHz
loop bandwidth, 60° phase margin, ICP 600 µA

1 ps
rms jitter target; 0.6 ps above 4 MHz

13 mW
the SMACD 2026 design draws 12.73 mW

Is –100.8 dBc/Hz the VCO or the loop?

A proven 4 nH tank, retuned to 2.5 GHz



4 nH
centre-tapped inductor, Q 16.8, on TopMetal2

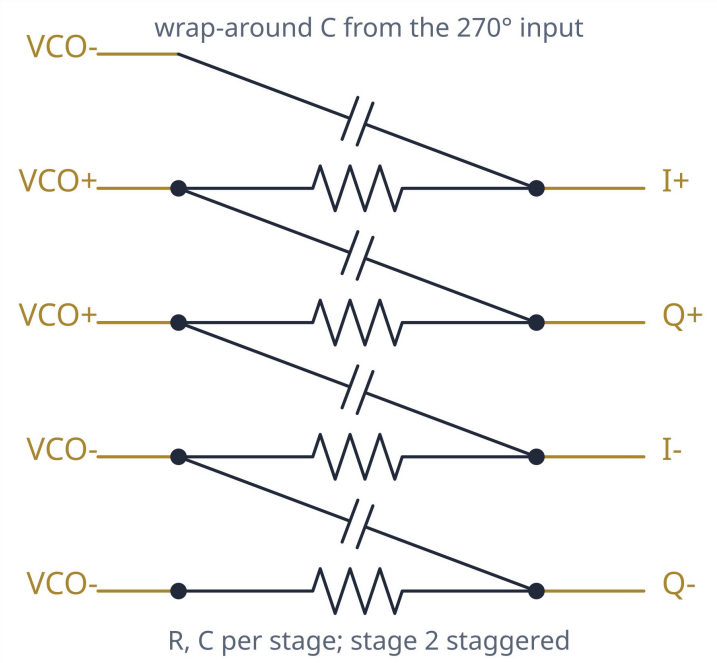
1.01 pF
total tank capacitance at 2.5 GHz, parasitics included

1.89 mS
minimum gm for start-up against a 1.06 kΩ tank loss

±10 %
tuning from varactors plus a 3- to 5-bit MIM bank

Retune from 2.4 GHz by removing 86 fF.

An RC ring makes four phases 100 ps apart



2 stages
RC poles at 2.0 GHz and 3.1 GHz

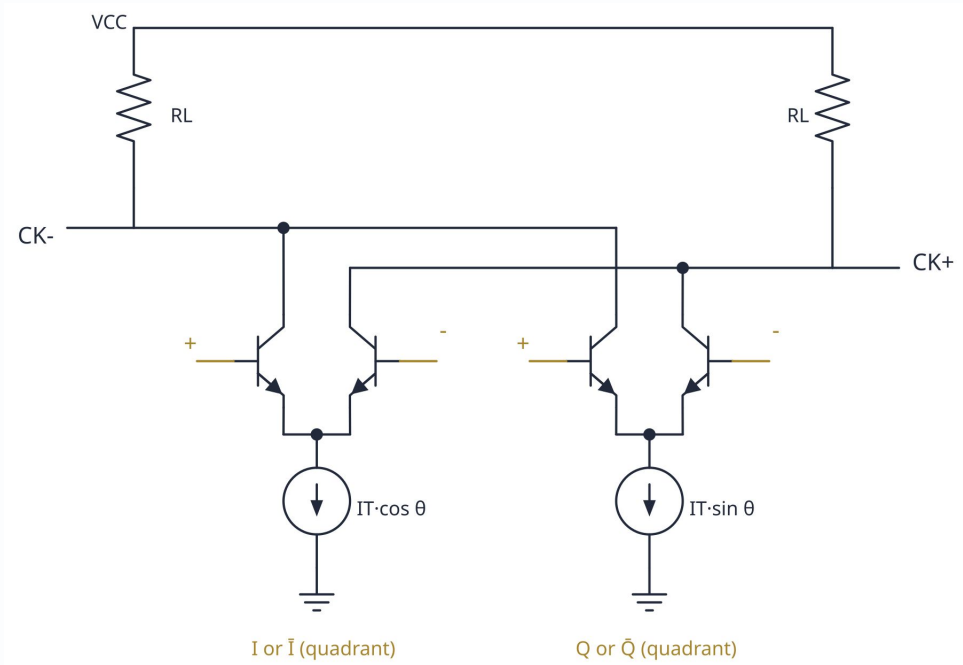
0.07 dB
I/Q amplitude imbalance over a ±20 % RC spread

0.6°
rms phase error with 1 % mismatch; 1° is 1.11 ps

5.2 ps
clock-path DJ: I/Q 2.0, duty 2.0, PI 1.2, of 6 ps

Buffers and a duty-cycle corrector follow.

Two PIs move the samplers in 6.25 ps steps



6.25 ps
64 steps per 400 ps clock period

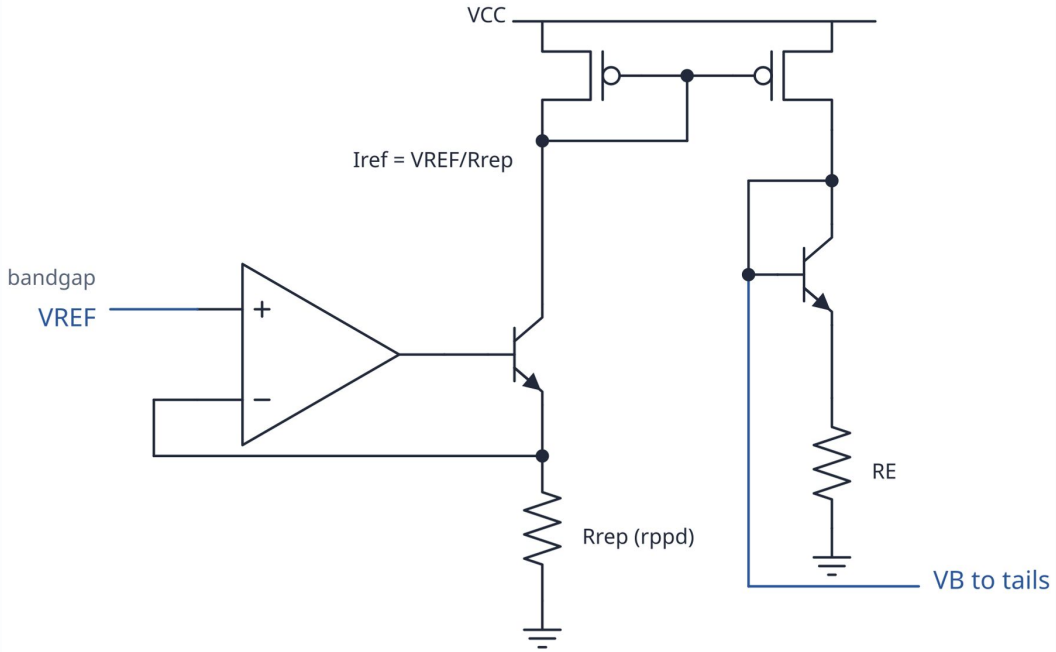
±0.6 ps
INL with sine/cosine weights; linear weights give ±4.5 ps

k, k+16
codes of the data and edge PIs, a quarter period apart

6–10 mW
for both PIs and their limiting buffers

The inputs must stay near-sinusoidal.

Tail currents track the load resistors



VREF/R

reference current from a replica rppd resistor

IT·RL

each swing becomes a ratio of like resistors

±20–30 %

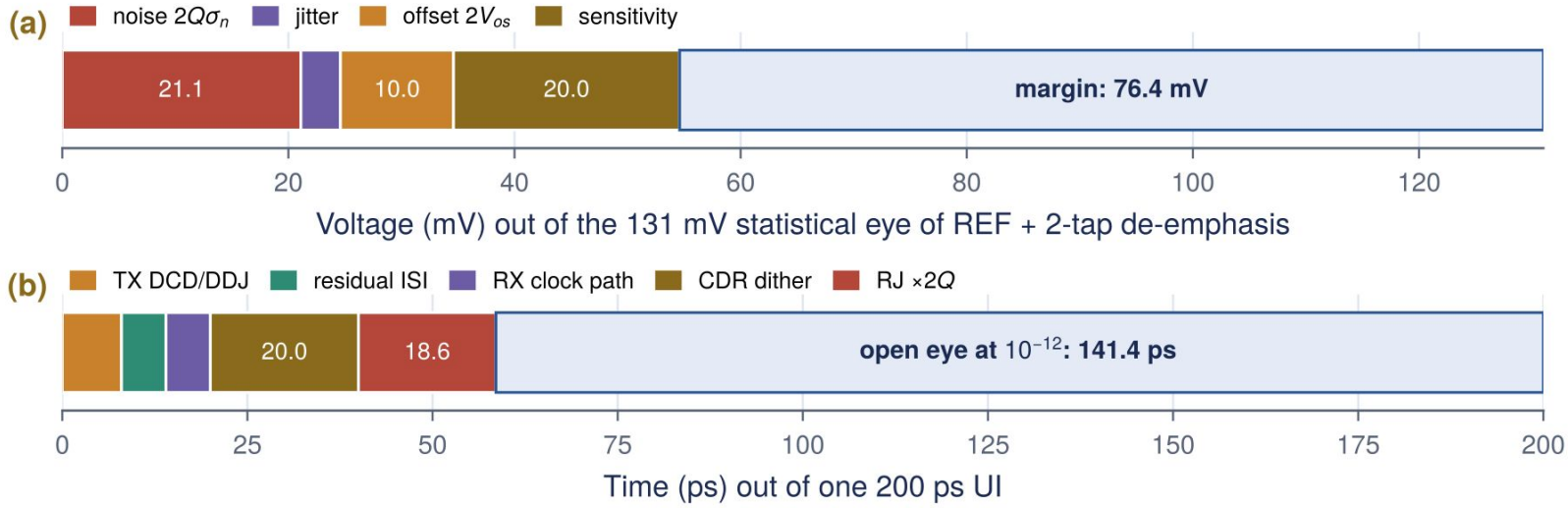
poly spread that the swings no longer follow

3-bit trim

kept on the driver: its 50 Ω line is off-chip

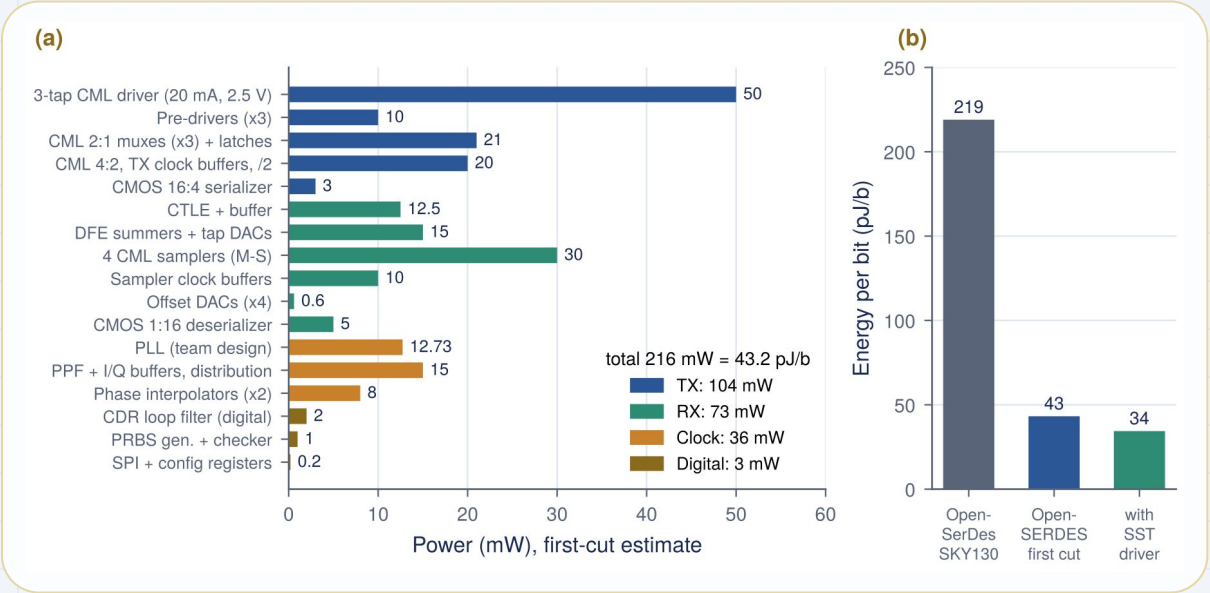
Decouple VB at every block.

Do the budgets close?



Voltage closes with 76 mV to spare. Timing closes by just 1.4 ps: it is the tight budget.

Where the 216 mW goes



216 mW
first-cut total for one transceiver

43 pJ/b
five times less energy per bit than the all-digital SKY130 OpenSerDes

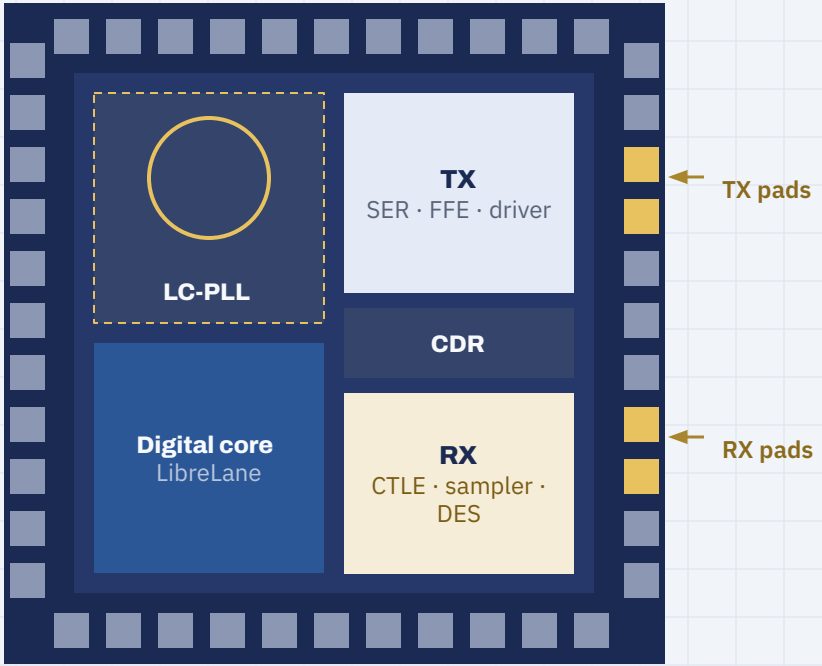
48 %
of the power sits in the TX, mostly static CML current

The CML driver is almost a quarter of the power. An SST driver brings the link to 34 pJ/b.

From the tutorial: Figure 14.8 · thebricd.org/serdes-tutorial

Floorplan concept

- Die of roughly [2 × 2] mm² in SG13G2 (to be sized)
- TX and RX pads on one edge, shortest bond wires
- LC-PLL in its own corner, guard ring, own supply
- Separate AVDD, DVDD and VDDIO domains
- Digital core hardened with LibreLane
- Seal ring, fill and logo from the template flow



Simulation testbench & sign-off



Sweeps

- Channel loss: 0 to [__] dB at 2.5 or 5 GHz
- PVT corners and Monte Carlo
- Jitter and supply-noise injection
- FFE, CTLE and DFE settings

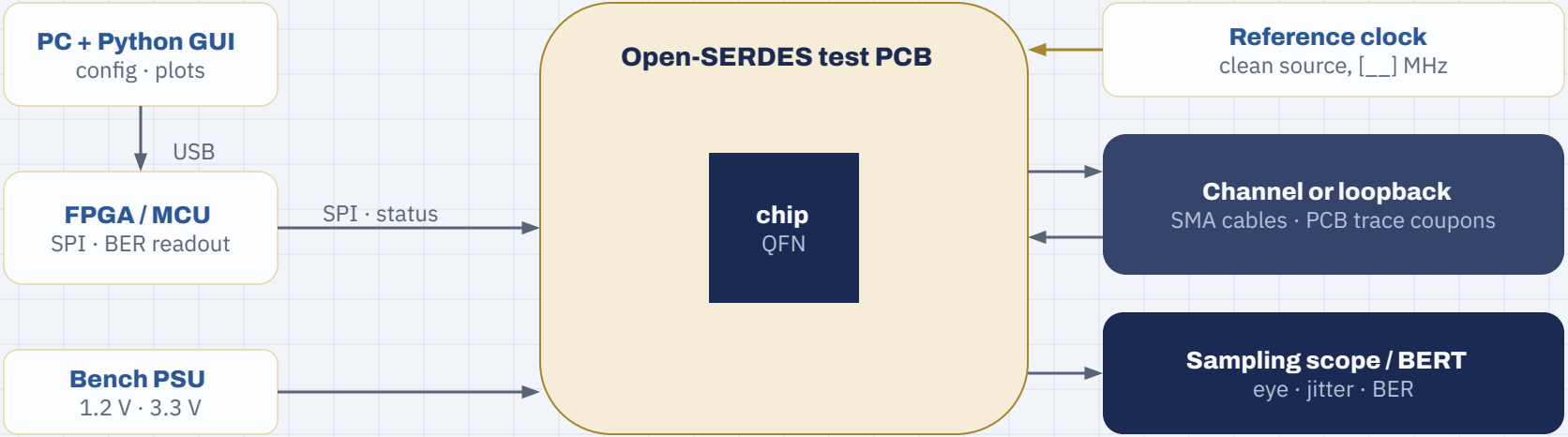
Pass criteria

- Eye height ≥ [__] mV
- Eye width ≥ [__] UI
- BER ≤ 1e-12 (statistical)
- Power ≤ [__] pJ/bit
- CDR lock in < [__] µs

Sign-off checks

- Full-chip DRC (KLayout)
- Full-chip LVS, no black boxes
- PEX and post-layout re-simulation
- CI regression on every commit

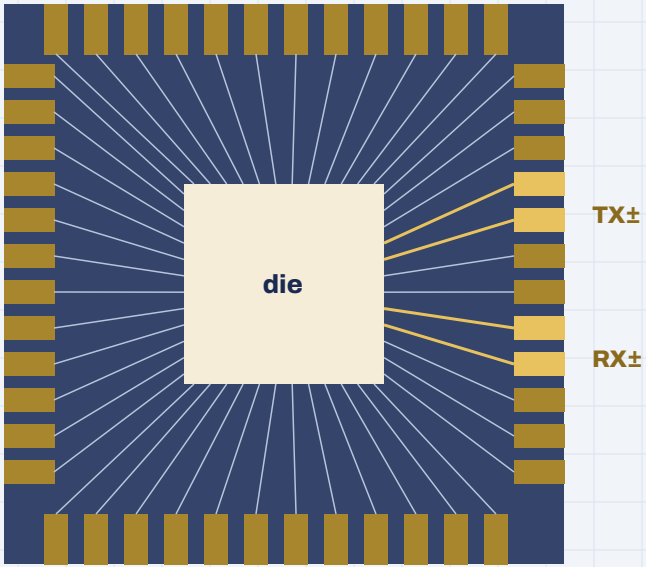
Test bench in the lab



WE WILL MEASURE

- Eye diagram
- BER bathtub
- Jitter (RJ / DJ)
- Power per bit
- CTLE response
- CDR lock time

Package & pinout (concept)



QFN-48, 7 × 7 mm (concept)

Group	Pins	Notes
High-speed	TXP, TXN, RXP, RXN	GSSG, shortest bond wires
Clock	REFCLK P / N	external reference
Control	SCK, MOSI, MISO, CS	SPI config + BER readout
Supplies	AVDD, DVDD, VDDIO, VSS	separate domains
Status	ERR, LOCK, DBG	debug and monitoring

Bonding plan generated from a config file, as in the JKU template flow.

PART 5

Roadmap & Community



Roadmap: blocks → 5/10 Gb/s → beyond

PHASE 0

Feasibility

- Channel and link model
- Pick the architecture
- Freeze block specs

PHASE 1

Building blocks

- 10 Gb/s-ready CML cells
- Driver, CTLE, sampler, 10 GHz VCO
- Test-chip shuttle

PHASE 2

5/10 Gb/s transceiver

- TX + RX + PLL + CDR
- 5 Gb/s pass, 10 Gb/s target
- Full-chip tapeout

First silicon

PHASE 3

Measure & publish

- Eye and BER in both modes
- Open measurement data
- Paper: JSSC / TCAS, SMACD 2027

PHASE 4

Beyond

- 16–25 Gb/s, quarter-rate
- Adaptive DFE, PAM4
- Multi-lane and chiplet links

Every phase ends with a tagged release: **design files, models and data, all open.**

Get involved

System modeling
Python / Julia link models, channels, the GUI

Analog & RF
CML drivers, CTLEs, samplers, PLL and VCO

Digital
SystemVerilog SER/DES, PRBS, CDR and DFE logic

Layout & EM
KLayout, Magic, openEMS, parasitic extraction

Test & measurement
Test PCBs, eye diagrams, BER

Docs & teaching
Tutorials, Quarto pages, GitHub docs

Interested? **bricd.org@gmail.com**

`https://github.com/bricd-org`

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11. IEEE 802.3cb (2.5GBASE-KX and 5GBASE-KR backplane Ethernet); Tiny Tapeout IHP shuttles, tinytapeout.com

These slides were prepared with the help of AI tools and may contain mistakes. If you find one, please email bricd.org@gmail.com and we will correct it.